Direct Frequency Synthesis for 47GHz transceivers

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Introduction

This paper will explore the options for deriving the fundamental oscillator frequency for 47.088GHz operations from a Direct Frequency Synthesiser (DFS) locked to a GPS source. Two designs will be explained as options for systems using a 144MHZ IF – frequency schemas for other options using 432MHz and 1296MHz IF's will also be proposed.

The work produced in this paper is further development of work already published by myself and others in earlier papers - see reference list.

Detailed circuit diagrams for the DFS are not included in this paper, since the most current information is available via my web-site, which has a resource section for the DFS projects – please visit http://g4hup.com/DFS/DFSdocIss2.htm.

Direct Frequency Synthesis

Direct Frequency Synthesis is a method of generating frequencies locked to a reference source by processes of multiplication, division and mixing – there are no feedback control loops, or comparators, and the quality of the output signal is directly determined by the quality of the input reference signal. Several single loop DFS designs have been published in amatuer literature (WA1ZMS et al) over the past few years, although the principle has been used for many years – since the days of vacuum tubes. Virtually all of these designs have been for 'single loop' solutions. The addition of a second divider and mixer loop considerably expands the frequency generation range (K3SIW, G4HUP).

G4HUP DFS PCB – Issue 2

Most of the known previous designs (except for F9HW) have presented single solutions,and no PCB's have been made available for general experimentation and construction – DFS's are by their nature very 'solution specific'. However, when converting the protoype 2 loop DFS into a PCB for WC8VOA, I decided that a flexible approach could be implemented which could serve as a basis for many different implementations – this gave rise to the Issue 1 of the G4HUP DFS PCB. Flexibility was provided in:

- the options for divider programming by jumpers
- the options for using LPF's or multipliers following each divider – jumper selected
- the option to multiply the first mixer output

- the use of 'standard' inductors, eg Toko S18, 10k's and Minicircuits mixers

The PCB has now moved to a new version, Issue 2, with some improvements to the filtering available, but considerable changes to the construction:

- easy implementation of screening between stages to reduce low level spurious products
- use of Toko 7KLL inductors, to eliminate re-winding of 10k's

The designs presented here are the first published to use the revised PCB.

47GHz Options

Table 1 shows the various combinations of common IF and LO multiplier chain factors for achieving an operating frequency centred on the 47.088GHz narrowband segment.

The table shows the starting frequency (Fundamental) for each case, and also highlights which are achievable with the DFS designs presented here. Note that no options with an IF of 2320MHz, or using a multiplier factor of 512 result in solutions that can be produced with the DFS. However, there are usable options for 144, 432, 1296 and even 2304 MHz IF's.

IF	LO Inj Freq	Multiplier	Fundamental
144	46944	384	122.25
144		432	108.6667
144		512	91.6875
432	46656	384	121.5
432		432	108
432		512	91.125
1296	45792	384	119.25
1296		432	106
1296		512	89.4375
2304	44784	384	116.625
2304		432	103.6667
2304		512	87.46875
2320	44768	384	116.5833
2320		432	103.629629
2320		512	87.4375

Table 1 – Frequency options for 47GHz LO
unsuitable options for DFS generation are greyed out

Table 2 takes the results from Table 1 and shows the DFS solutions only, in order of ascending frequency. These solutions are then analysed to show how they can be produced within the DFS – considering the input reference frequency (10 or 15MHz) and what the VHF multiplication factor is. In some cases there is more than one solution possible, so there may be several lines in the table for the same frequency. In such cases some solutions may be 'better' than others.

Single loop solutions are generally preferred, since the resulting output is inherently cleaner due to reduced mixing products requiring filtering, so these are shown on the white background – essentially the 106 and 108MHz options, for 1296 and 432MHz IF respectively, both using a 432 multiplication factor in the LO chain, and the 108.6667MHz solution for a 144MHz IF. The remaining synthesisable solutions are all two loop implementations.

To decide which solution to choose from several there are some obvious considerations:

- The lower the VHF frequency, the higher amplitude from the multiplier (ie less gain is required)
- The higher the frequency that must be added to the VHF frequency, the further way the image – so the filtering is easier
- Avoid solutions where the MF and LF loops have almost the same frequency if possible –eg 103.667MHz with either 7 and 6.667MHz or with 3.333 and 3MHz mixes. The 12 + 1.667 is the best solution of this group.

Frequency (MHz)	Ref i/p	VHF mult	MF loop	LF loop
103.6667	10	90	7	6.6667
103.6667	10	90	12	1.6667
103.6667	10	110	3.3333	3
106	10	90	16	
106	10	110	4	
106	15	105	1	
108	10	90	18	
108	10	110	2	
108	15	105	3	
108.6667	10	110	1.33	
116.625	10	110	6	0.625
119.25	10	110	8	1.25
121.5	10	110	4	7.5
121.5	15	105	9	7.5
122.25	10	110	6	6.25
122.25	10	130	4	3.75

Table 2 – DFS solutions for the useful options from Table 1
unshaded lines show 'preferred' single loop options

Although solutions are shown for a 15MHz reference input, there is no advantage, in this case, compared to using 10MHz inputs as far as complexity of the DFS implementation is concerned (unlike the 106.5MHz solution for 10GHz). However, there may be advantages in that less gain is required, since the VHF multiplier is only at 7 times, instead of 9 or 11, and this should contribute to a lower noise at the output.

Degradation due to Multiplication

Of course, the quality of any source, in terms of the spurious products, will degrade when it is multiplied in frequency. With the DFS solutions shown, it is relatively easy to achieve a level of -65dBc for spurii, and with care, levels approaching -70dBc are possible. This will be degraded according to the formula $D = 20\log_{10}N$, where N is the multiplication factor – Table 3 shows the degradations to be expected. So we can expect a spurious output at -70dBc to give a level of -17 or -18dBc when multiplied up to the final frequency for LO injection?

Multiplication Factor	Spurii Degradation (dB)
384	52
432	53
512	54

Table 3 – Degradation of spurii for given multiplication factors

This would certainly be true, but for two factors:

- The multiplier chain has filtering and frequency selection – this will reduce the level of these products, especially those that are not close to the wanted frequency.
- Due to the multiplication process, such products are widely spaced at the final frequency – if we assume a multiplication of 384, then a product 250kHz away from the wanted fundamental frequency will be 96MHz away at 47GHz.

Taking these two effects into account, the levels of the spurii at 47GHz will typically be around -35dBc or better, and are unlikely to be close enough to the frequency of operation to cause any problems to other operators and services, or to cause the user problems due to reciprocal mixing or other excess noise paths into the receiver.

Specific Solutions

Two implementations will be outlined here – a single loop solution for 108.667MHz, and a two loop solution for 122.25MHz – both of these are for

operation with a 144MHz IF, and provide good examples of each type of implementation.

Note that the circuit schematics are not published here, since they are available from the DFS website at http://g4hup.com/DFS.html.

Single Loop 108.667MHz DFS

The configuration schema for this design is shown in Fig 1 – the design is interesting since although it is only a single loop solution, it requires both a low pass filter and a multilpier stage from one of the available sets. The multiplier is used to double the 10MHz to 20MHz – this can then be divided by 15 to derive the 1.33MHz signal.

Based on earlier work, the more traditional approach would have been to divide the 10MHz by 5, down to 2MHz, then multiply this up to 4MHz. Dividing this by three would give the wanted 1.33MHz. However, since there is no need for the 2MHz signal to be present, it is probably better to avoid generating it – it is one less low frequency signal that must be filtered out.

There would be no problem in taking the 1.33Mhz directly to the mixer after the jumper at SJ902, but given that the image is only 2.667MHz away, the opportunity to use another stage of band pass filtering is recommended, to clean the signal up before mixing with the VHF output.

Note that lines shown dotted on the diagrams indicate 'cut & strap' on the PCB

Fig 2 shows the physical implementation, and Fig 3 shows the output spectrum currently achieved

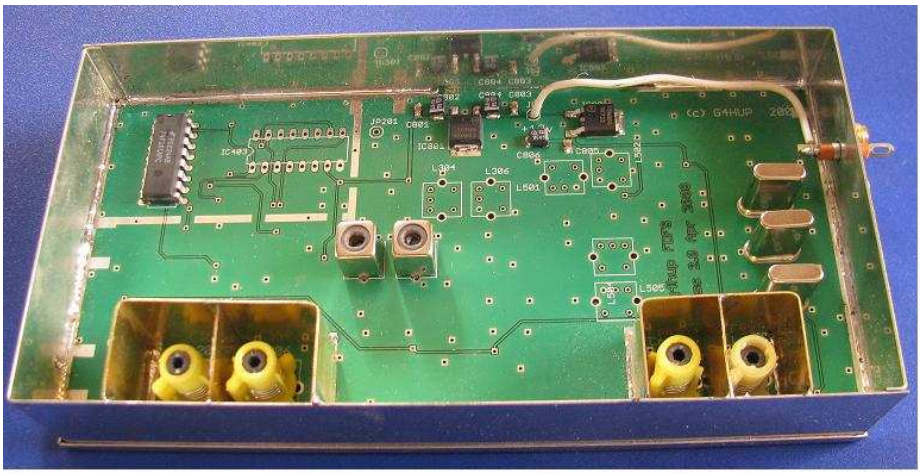
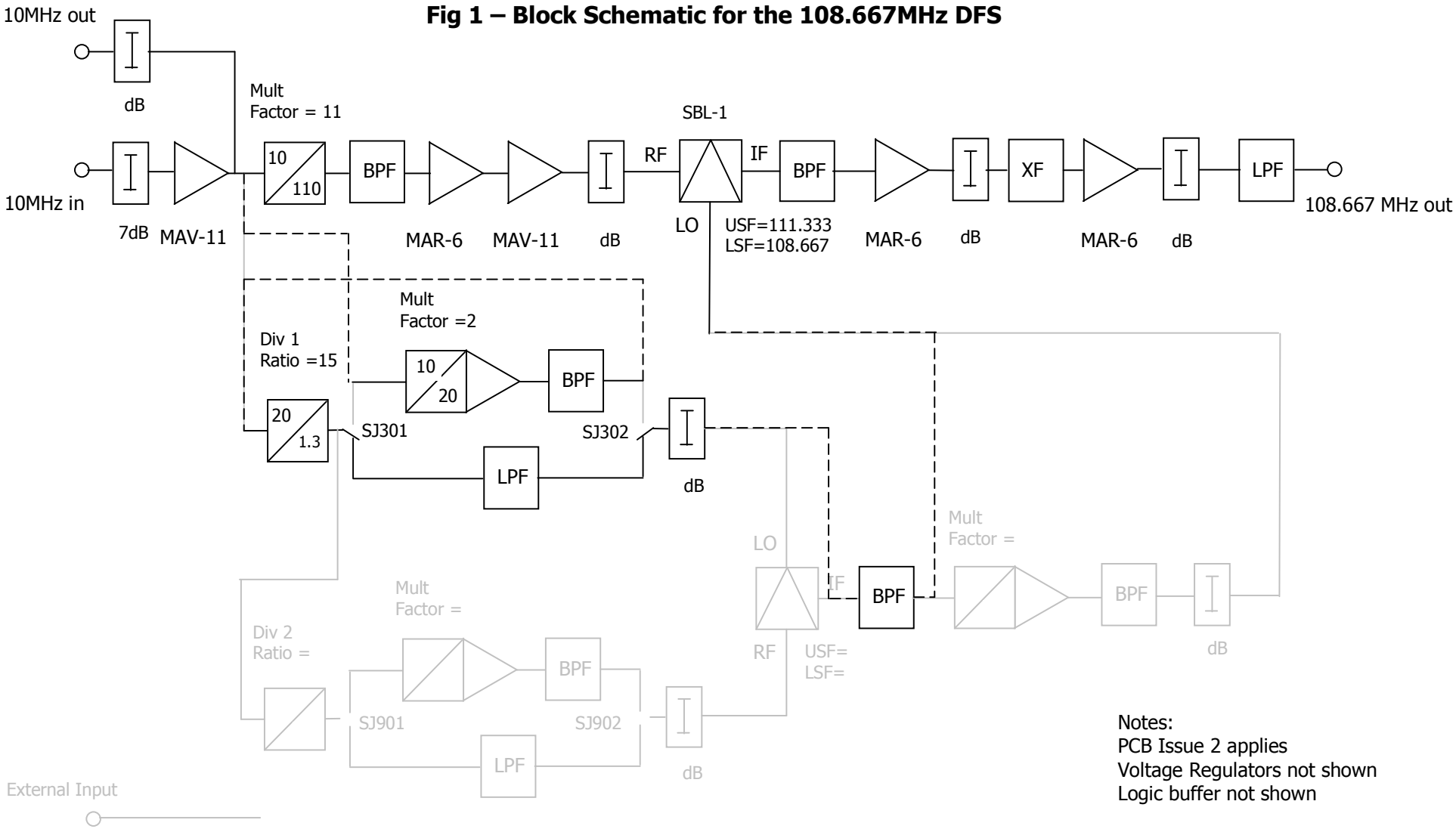


Fig 2 – 108.667MHz DFS solution

Fig 1 – Block Schematic for the 108.667MHz DFS



G4HUP Direct Frequency Synthesiser Configuration

Version: 108.667MHz

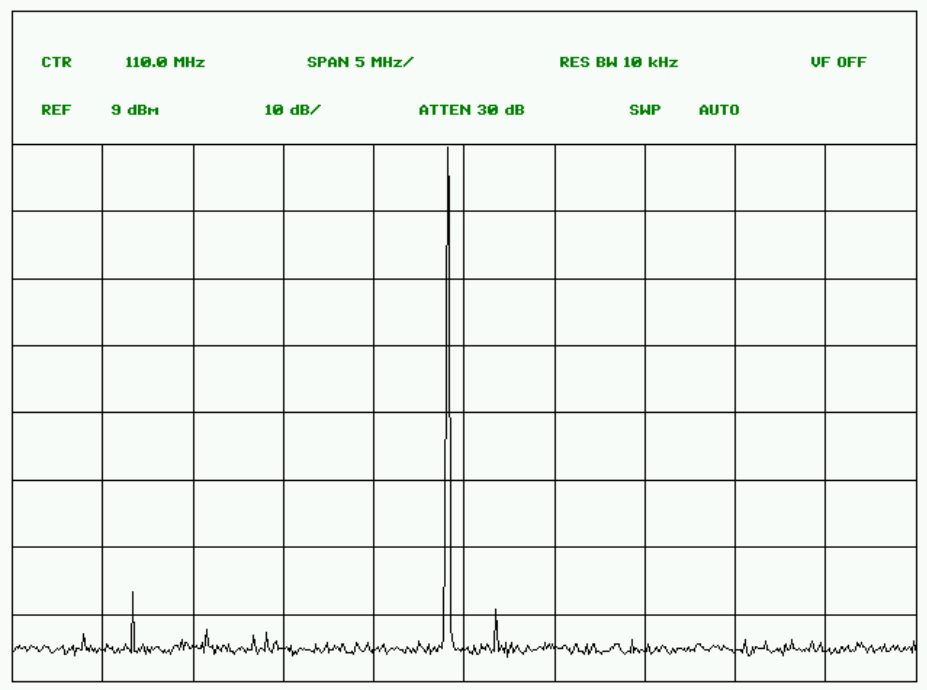


Fig 3 – 108.667 DFS output spectrum

Ther are two notes to be added to what you see in Fig 3 – it is obvious that there are two significant spurii visible at approx -66dBc and -70dBc. The lower frequency spurious is in fact the 90MHz VHF multiplier output. The -70dBc product, close to the wanted signal is the upper side frequency of the mixer, and is thus 2.6667MHz away from the wanted signal. No screening has been put into this version, since so far it is for demonstrating and showing – the 90MHz signal should reduce noticeably with the addition of screens. However, the mixer product is unlikely to be improved by anything other than tighter filtering. On a further note, the construction of the version on which the measurements have been made did not include the post-mixer BPF in the 1.33MHz path that is shown in Fig 1

Performance of the 108.667MHz design

The 108.667MHz design detailed here has been built and has given a set of results (Table 4) commensurate with the previously achieved measurements.

Parameter	Measured Value	Units/comment
RF output level	+7	dBm
Spurious Products	-67	dBc
Harmonics (2f)	-42	dBc
Icc	360	mA@ 13.8v DC

Table 4 – 108.667MHz DFS Performance – measured results

Two Loop 122.25MHZ DFS

This version, shown in Fig 4, uses multipliers in both the MF and LF paths. The 10MHz input is multiplied by 11 to 110MHz for the VHF signal. Additionally, it is also divided in both divders in parallel. Dealing first with the MF path it is divided by 5, to 2MHz then multiplied by 3, to give 6MHz. In the second, LF path, it is divided by 8 to give 1.25MHz, which is then multiplied by 5 to give 6.25MHz. The USF from the mix of these signals is filtered and amplified at 12.25MHz before being mixed with the 110MHz signal, giving a USF of 122.25MHz.

Whilst this is not perhaps an optimum mix, since the two MF signals are very close in frequency, there is little to choose between the options for generating this frequency. The alternative is to generate 130MHz in the VHF multiplier, and subtract 7.75MHz from it. Here again, the MF products are only 250kHz apart – exactly the same spacing. Given that the 110MHz option will require less gain in the VHF amplifier path before the mixer, then the method shown is probably the better overall solution.

Filter Implementations

With the advantage of previous developments, filter designs for the 108.667MHz version already exist – from the DFS Filter information at http://g4hup.com/DFS/DFS Data.html the 4MHz filter from the 94.667MHz version can be used, and the 1.5MHz filters (F3 from 92.25MHz and F6 from 106.5MHz) will tune down to cover 1.33MHz.

For the 122.25MHz DFS, filters are needed at 6.00MHz, 6.25MHz and 12.25MHz. A common design will suit the 6 and 6.25MHz requirements, and the 11.75MHz design (F6 from 101.75MHz) will tune 12.25MHz. Hence the only new filter required is to cover the 6MHz part of the design. Fig 5 below shows a proposal on which such a circuit could be based, whilst Fig 6 shows the simulated frequency response

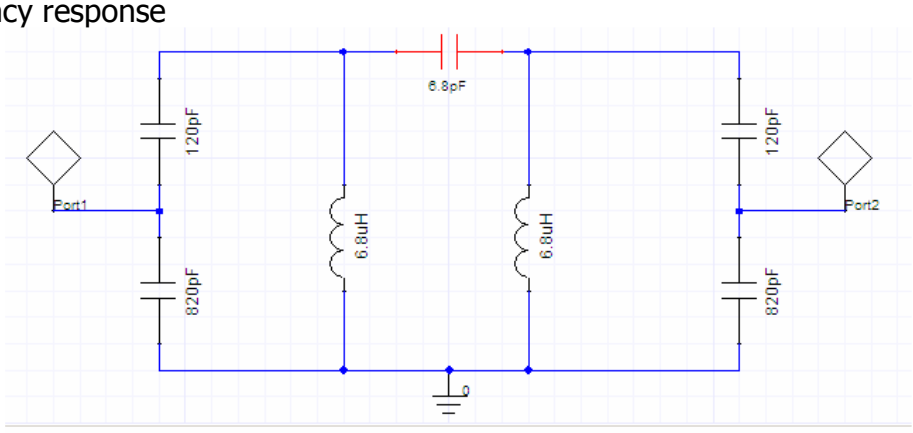


Fig 5 – 6MHz Band Pass Filter circuit schematic – Ansoft simulation

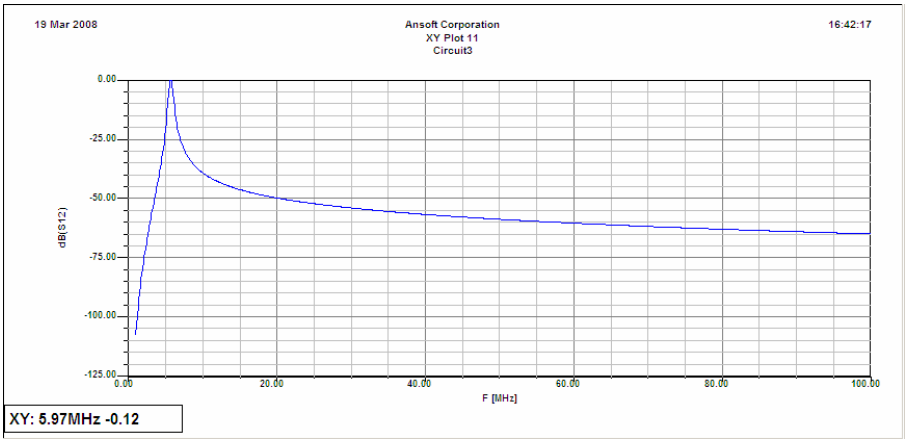


Fig 6 – 6MHz Band Pass Filter Response – Ansoft simulation

Output Filtering

A common requirement of all DFS designs is the need to clean up the output before injecting into the multiplier chain. Three stages are availble in the PCB design:

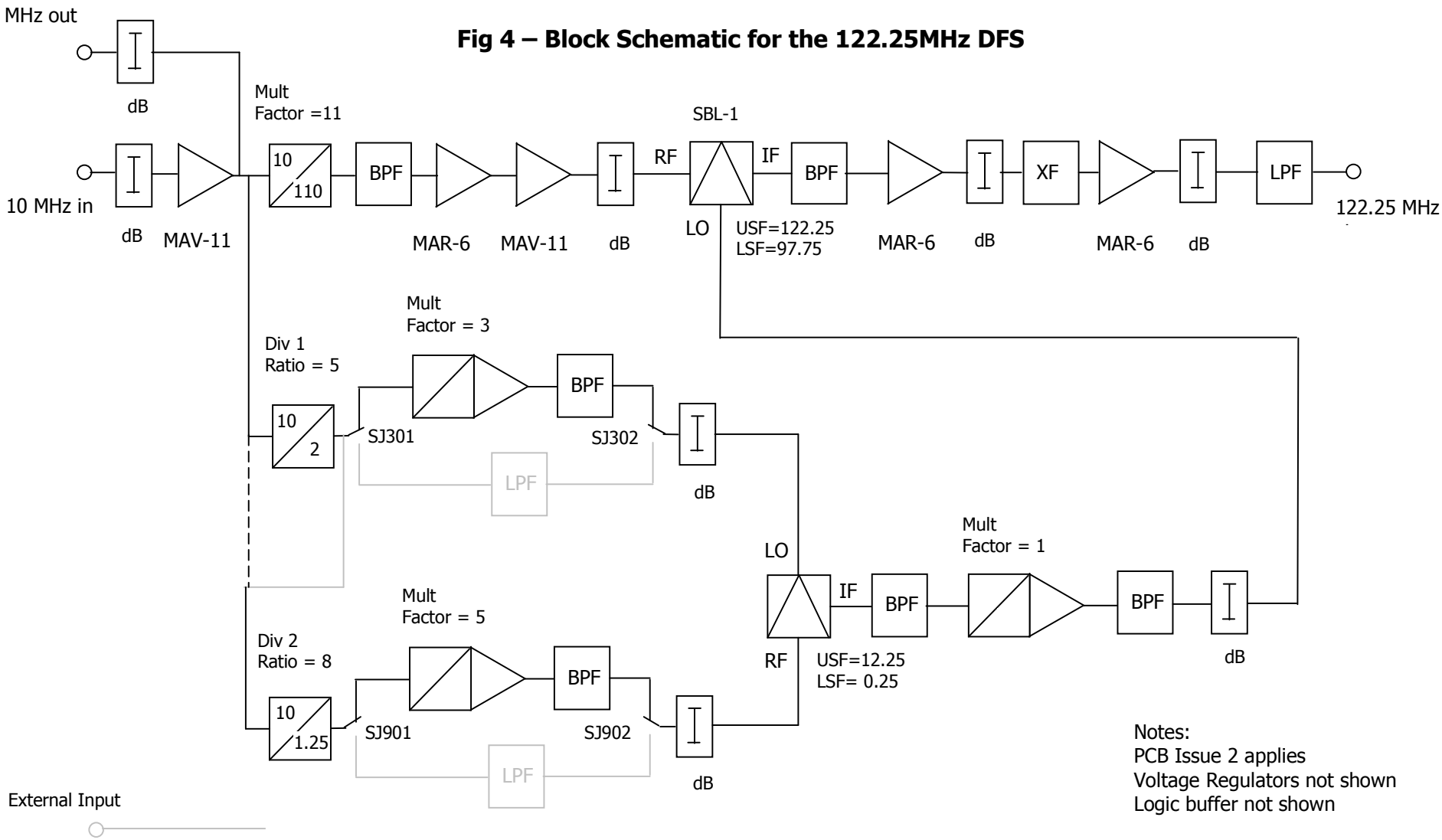
- A BPF follows the VHF mixer to select the wanted side frequency
- A VHF crystal ladder filter reduces close in products around the wanted frequency
- An LPF on the output reduces the levels of harmonics.

It is recommended that all of these filter options are used.

The crystal filter requires three 5th overtone crystals at the output frequency. In the current implementation these are series resonant, room temperature types in a standard HC49/U holder. Since these are being used as filters, rather than in an oscillator function, the requirements (and therefore the cost) are more relaxed. Should the operating temperature of the DFS change, the effect of the change on the crystal filter operation will be a small decrease in output level only.

A word should be said here about aligning the crystal filter, based on the experiences of DFS constructors. It is not possible to align the filter by using 'maximum smoke' techniques! Whilst this will give minimum loss through the filter, it will also fail to give the best rejection of the low level, close-in products. It is essential that this filter is set-up for best rejection and balance of the unwanted signal components using a spectrum analyser.

Fig 4 – Block Schematic for the 122.25MHz DFS



G4HUP Direct Frequency Synthesiser Configuration

Version: 122.25 MHz

Conclusions

The two designs presented here represent options which can be used to ensure that a 47GHz transceiver is locked accurately in frequency – a significant contribution to terrestrial or EME operation. Other options exist, as presented in Table 1, for using other IF's or multiplication factors. Some stations, of course, use seperate transmit and receive multipliers – a DFS at 109MHz will give 47.088GHz with a 432 times multiplier. Starting from 122.625MHz will need a times 384 multiplication – this latter frequency is not so easily synthesised in a DFS, but can be produced in two loops using either 110 or 130MHz as the VHF chain.

Direct Frequency Synthesisers are not the only method of achieving frequency lock for these higher bands, but their inherent simplicity, in regard to the method of generating the output frequency, and the absence of feedback and control loops, can make them an attractive alternative to PLL's and their variants

The G4HUP DFS PCB's make experimentation with different frequency schemas relatively easy, due to the versatile options available on the board – however, the completed unit is a fully functional part of the station, rather than a 'prototype' unit. Additional frequency converters (10 to 15MHz) and multipliers (doubler/tripler/quadrupler) are also available, via the website.

References

WA1ZMS, F9HX, G4DDK, WW2R, K3SIW – previous amateur DFS papers – all available at http://g4hup.com/DFS/DFSdoc.html

Flexible DFS resource site – http://g4hup.com/DFS/DFS.htm

PCB's, kits and ordering – http://g4hup.com/Orders.html